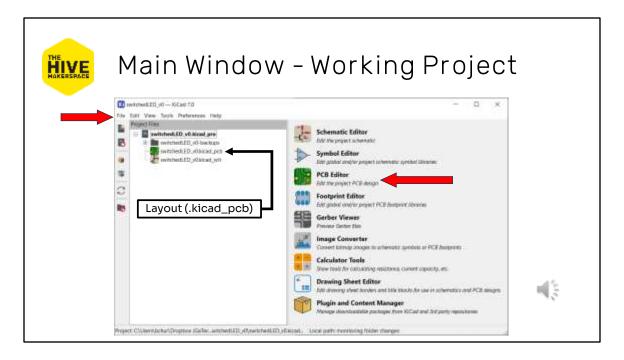


Hi all, welcome to The Hive's series on PCB Design with KiCAD. My name is Ben Hurwitz, and in this series, we've been walking through the PCB design process using KiCAD as our electronics design software.

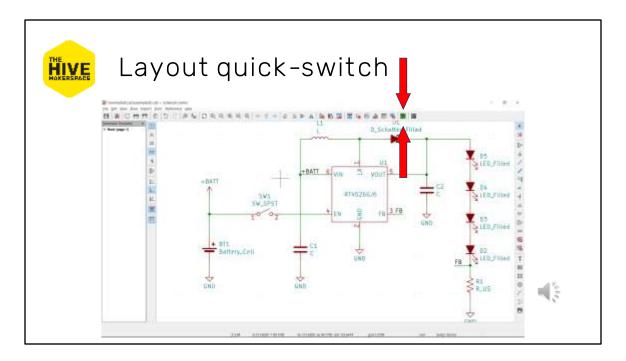
In the last video, part 4E, we finished off the schematic capture with a look at the ERC, or the electrical rules check, and a few bits of schematic miscellany.

In these next few videos, we'll shift focus to the layout portion of the design process, which KiCAD calls the PCB view, in which we'll actually physically align and orient the actual components on the board and connect them with traces.

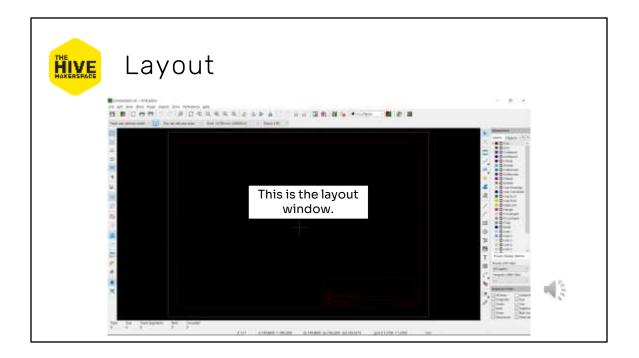
This section, part 5A, will introduce the board editor and look at setting up the board's defaults and design rules. Let's get started.

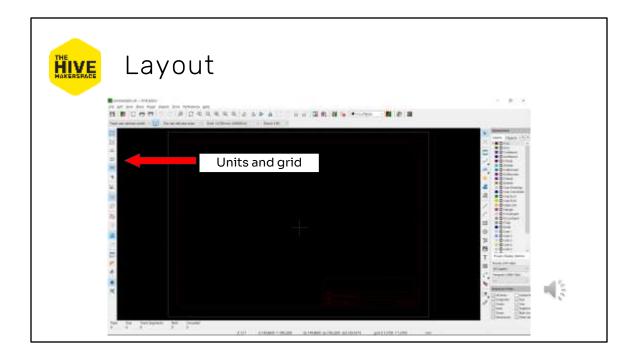


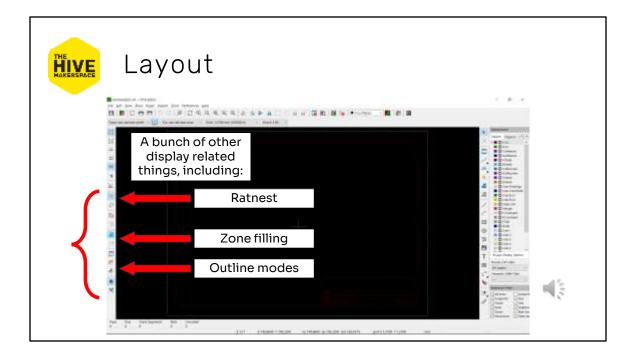
If you're just opening KiCAD for this video, go ahead and *load the project via the "File" menu, and open the PCB editor by ether *double clicking on the layout file with extension .kicad_pcb, or by *clicking on the PCB editor icon on the right, which will open the current project's board view by default.

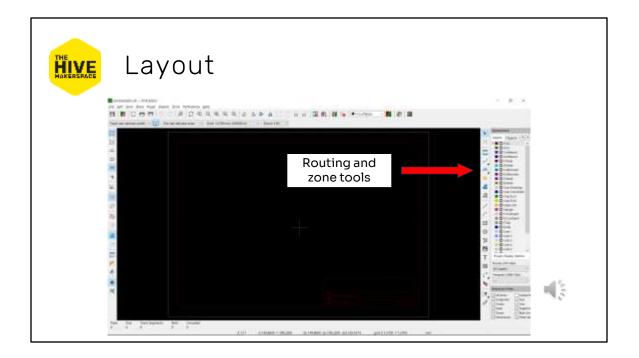


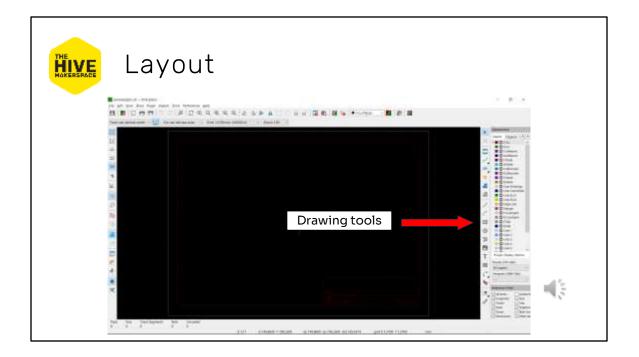
If you're coming from the previous video, part 4E, or you have the schematic editor up for whatever reason, you can also use the icon highlighted here to open the PCB view.

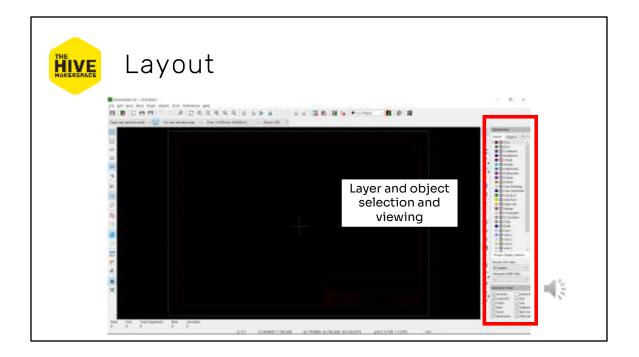


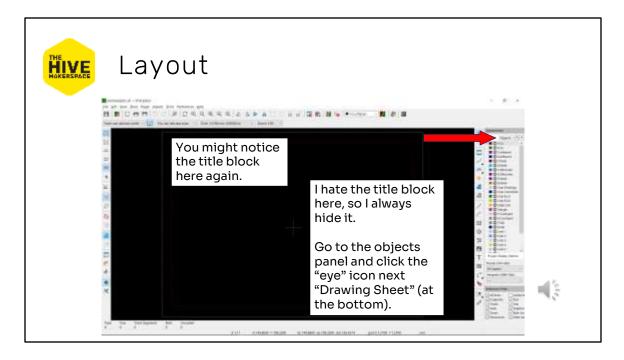




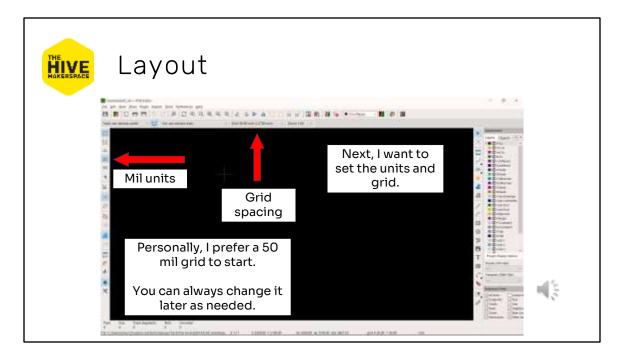




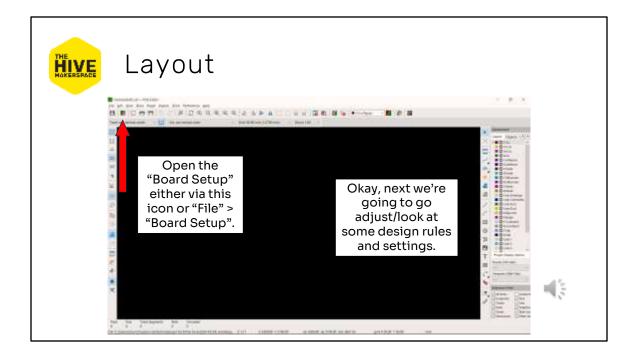




Similar to the Schematic editor, removing the title block requires making a new drawing sheet, which is beyond the scope of this tutorial.



Unlike the schematic in which the grid is really important to KiCAD's functionality, the grid is highly flexible in the layout editor, and can (and often will) be changed frequently.



HIVE Lay	out -	F	Board Set	nin	
HAKERSPACE LO Y				άp	
The "Board setup"	Board Setup				
window offers you	Hourd Eattor Laven				Add Liver Defined Layer.
many settings to	Physical Stackup Board Finish Solder Mask/Partie	P	FCourtyard FFab	Off-board, testing Off-board, manufacturing	
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	Text Variables	E4	# Sullexment	On-briatti, non-copper	
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important to		2	8.Paste	On-board, non-copper	
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of these settings in			B.Fab	OP-board manufacturing	- 16
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You can select/deselect	Formatting Text Variables Design Rules Comptiants	N N N	E Paste E Salkocrawiy E Musik	On-board, non-copper On-board, non-copper On-board, non-copper	
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they're deselected,			8.Reb II.Courtaind	OF-board Harufacturing OF-board, testing	- 1 k
versus just not being visible.			EdgeCuts	Board contour	40
	Import Settings from A	violte	r Boord.		QK Galon

This can be useful if it's important that you don't put silkscreen or copper on the backside of the board, for example. By removing them from the layers entirely, you minimize changes of error. You can also add user-defined layers here if you want or need, perhaps for a custom assembly process, required by your fab house, or for specific additional information.

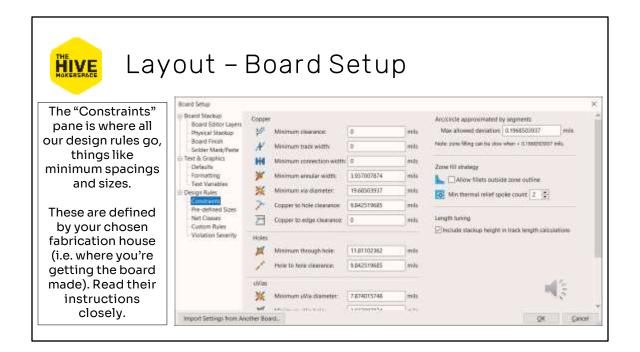
"Physical stackup"	Board Setup	South Contract		ver over these				2
refers to the the physical (rather than digital) layers	Board Editor Layers Brywal Klankte Board Finish Solder Mask/Parte	Copper layers (2 Layer 10 FSclocreen	Type Top Silk Screen	Material Not specified	Thionesi	Color	11222	Loss Tar
of the boards.	Test & Graphics Defaults Formatting Test Variables	FPaste	Top Solder Paste Top Solder Mask Copper	Not specified	0.1937007874 mil	Not specify	ed = 3.3	D
This is where you would set your	E Design Rules	Dielectric 1	Core – Copper	FR4	39,4488189 mill 1,377952256 mill	🗋 🚺 Not specify		0.02
board to be 4 layers, or 8 or whatever, using the	Custom Rules Violation Severity	ILMask ILPaste ILPaste	Bottom Solder Mask Bottom Solder Parts Bottom Silk Scener	Not specified	6.3937007874 m/	Not specifi		0

You can do some really advanced setup in here, though I'm honestly not sure how much of it is used in other parts of the software versus just being for your (and you boss's) knowledge.

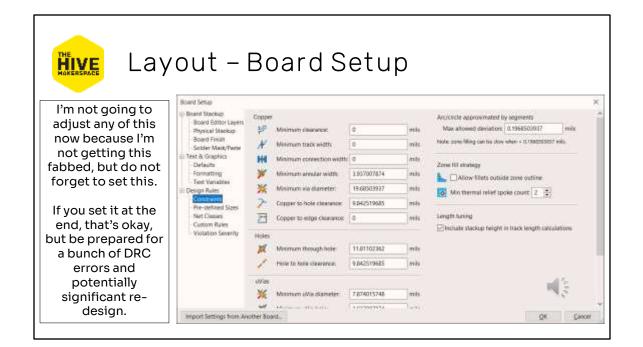
The units in this pane and in all other panes are derived from the units specified in the main layout editor window. KiCAD is a metric-based design tool, which is why the values are so wonky in mils.

Lay	out –	Вог	ird Setu	p					
Here you can set some defaults for text and graphics.	Board Setup Board Stackup Board Stackup Physical Stackup Board Finish Soliter Math/Parte	If Stackup Cafead properties for new graphic lemit. Use Teators Teat Wattin Teat Height Teat Thickness Italic Keep Upright some Stackup and Fiscal Stackup Stackstrast Stackup Stackstrast Teat Thickness Italic Keep Upright Stackstrast Fiscal Stackstrast Stack							
The defaults are normally okay, but it can be hard to gauge what size you need.	Text & Graphics Contract Formathing Text Variables Constants Pre-stefined Sizes Net Classes Outron Raile Violation Severity	Edge Cutt Courtyards Fab Layers Other Layers Default propert Units Units	1.957007874 m 1.546503937 m 1.937007874 m 39.37007874 m 39.37 5965511811 m 39.37007874 m 39.37 bes for Here dimension objects: Automate		Outpoor -				
Good rule of thumb is that height = width = 6*thickness.))	Pressure Suppress trail	0.0000 ~	Arrow langth Arrow langth Extension line dfla	50	nin mit M			
]	Import Settings from A	nother Board.				C Garcet			

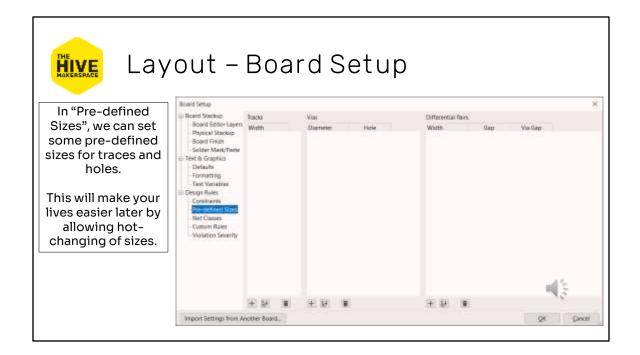
It can be a useful exercise to make a dummy layout only with text on it at various height/width and thickness ratios for your reference. If you print that board (CTRL + P, or "File" > "Print"), it can be handy to keep nearby for scale.

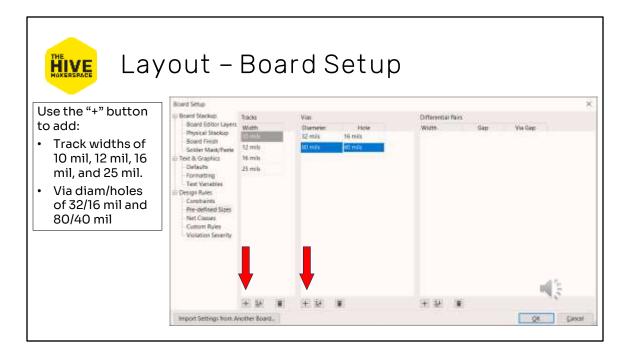


Many fab houses have software-specific instructions these days. Read them carefully! This is an easy way to make your design un-fabricatable, and require re-doing the layout.



Lay	out –	Board Setu	р				×
You can adjust the	Board Stackup	Dectrical					î.
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	Solder Mask/Perte	Overance violation:	(Error	Owning	Olgnow		
error, or ignore)	Text & Graphics	We is not connected or connected on only one layer	() Error	(# Warning	Olanave		
under the	Defaulto	Track has unconvected end	OEmpl	· Warning	Olynew		
"Violation Severity"	Formatting Text Variables	Thermal relief connection to zone incomplete:	(Error	Owaming	Olgnew		
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may end up with a		Micro six drift out of range:	(# Srar	OWening	C lignaria		
		Courtyands overlag:	(# Error	OWarring	C Ignate	46	
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		Footprint has malformed courtyant	@ Errer	OWening	C Ignaw	460	
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The parameter "diameter" for holes and vias refers to both the drill hole diameter itself plus the annular ring. It's generally a good starting point to have the ring diameter to be twice the hole diameter, and larger can make soldering easier.

These default values are not required by anything.

I like to keep my traces above the minimum allowable if possible, which is normally around 6 mils, to reduce the possibility of broken or damaged minimum-width traces that are more likely to have issues. For signals, I try to use 12 mils generally and neckdown, meaning shrink briefly, to 10 mils. Power traces should have the largest reasonable width possible. 25 mils is a good balance, and according to the tracewidth calculator at Advanced Circuits, can be used to pass 1A on external 0.5 oz copper with just a 10 degree Celsius rise in temperature. 16 mils is a good necking size for brief lengths over which 25 mils can't fit.

For the vias, the 16 mil diameter hole for vias is a classic default, and is good for small currents and signals. The 40 mil hole is about 1mm, and will fit a standard pin header if you need a via but do not have electroplating. It's also good for a lot more current. Not necessary typically, since you can use multiple small vias instead of one large

one.

Lay	out –	Board Setu	qL	
You can group nets together into <i>netclasses</i> to give them all the same default settings.	Bland Setup Bland Setup Bland Solor Layers Physical Stackup Bland Finish Solder Marky Partie Solder Marky Partie Text & Graphics Oxfaults Formathing Text Venables		la Son Via Hole "Wa Son	Wa Hote DP Wattin DP Ge
This is very useful if you want all your power traces to be	Design Rules Combaints Pre-defined Sizes Carton Rules	- - *		,
wide, or some traces to be very narrow.	Vialution Severity	Netclass assignments Patlarm	Net Cam	
		主 重		46
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	La	yc	out –	Bo	ard	Se	tup)				
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*Clearance... blah blah blah....

For The Hive's tool, because we don't offer a protective soldermask layer, it's important that this clearance is set quite large, 30-50 mils, to reduce the chances of accidentally jumping traces or a plane when soldering.

The uVia, or microvias, are extra-tiny vias that are typically used with BGA-style components with high-density ball-style pads underneath the package. These will add to your board cost, and are usually not needed unless you really can't find an alternative package.

DP stands for differential pairs, which are used when impedance matching is important, like for USB data or antennas.

Lay	out –	Board	Setup	0	
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Must be one pattern per assignment line.	Text Variables Design Rules Constraints Pre-defined Sume Net Obses Castum Rules Violation Severity	+ II			
ALT+Tab into the schematic to double-check the names.		Patters DATE GAD	_	Net Class Prover	Nets matching '+BATT' +BATT Click OK when you're done.
	Import Settings from A	Unother Board.			QK Cance

Netclass assignments can actually also be defined in the schematic by right-clicking a node or net.



And that ends part 5A of the KiCAD design tutorial series in which we introduced the layout editor and a number of pre-layout board setup settings. A PDF of this video is available as well, linked in the description and hosted on The Hive's Wiki.

In the next video, part 5B, we'll go through placement of the components and routing. See you then.