

Hi all, welcome to The Hive's series on PCB Design with KiCAD. My name is Ben, and in this series, we've been walking through the PCB design process using KiCAD as our electronics design software. Part 5, where we are, is focused on the layout portion of the design process.

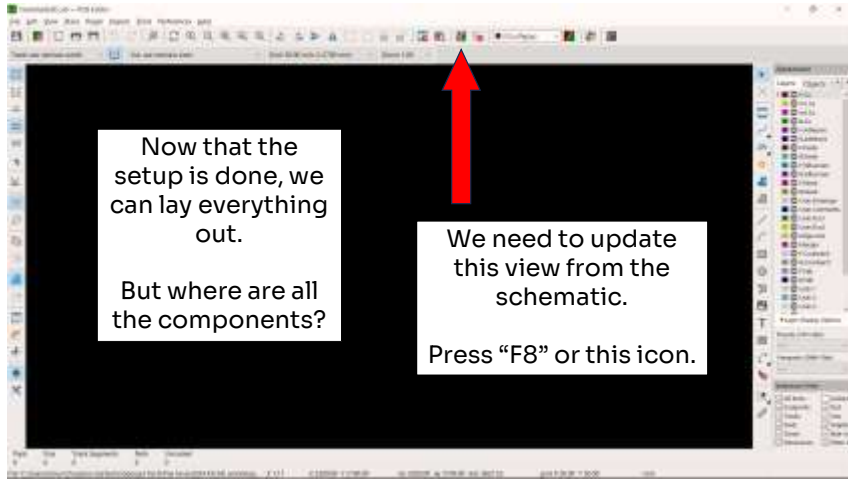
In the last video, part 5A, we introduced the layout editor, also called the PCB editor, and how to setup your design constraints and sizings.

In part 5B, I will take you through the basics of placing your components, called placement, and connecting them together, called routing. This video will primarily be focused on showing you the gist and then having you do most of these processes, so definitely follow along and pause to do the work.

Let's get started.



Layout



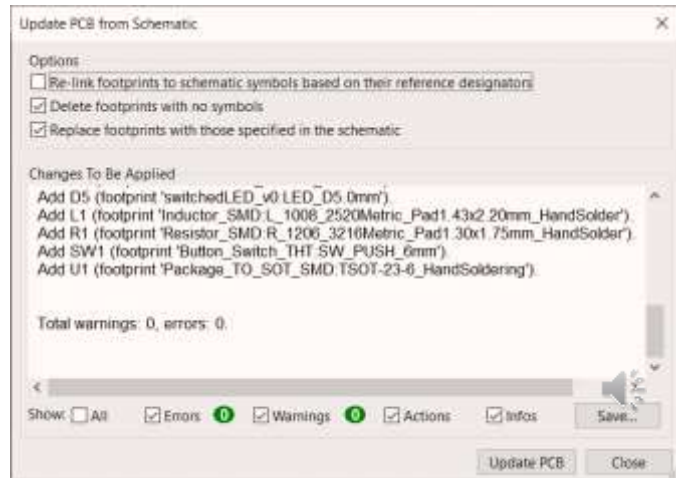


Layout

It'll take a second, but you'll get this window.

It will list the changes to be applied, which you can read through.

Click "Update PCB" to bring the footprints into the layout view.





Layout

Well phooey. We got some warning and errors.

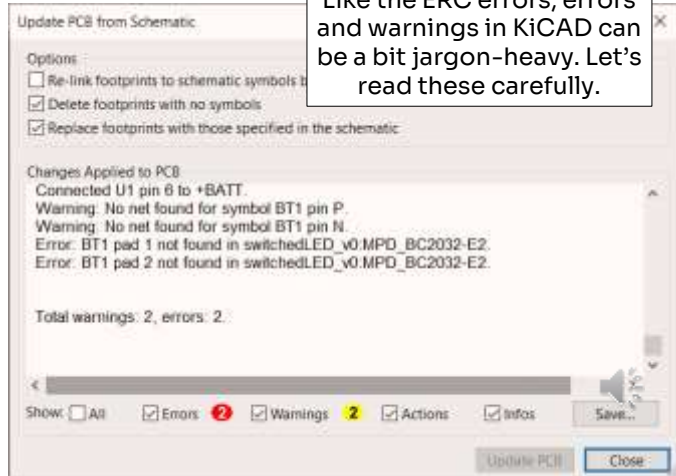
What are they?

The warnings say that the battery symbol (BT1) has no nets connected to its pins P and N.

The errors say that the BT1 footprint does not have a pad 1 or a pad 2.

.... What?

Like the ERC errors, errors and warnings in KiCAD can be a bit jargon-heavy. Let's read these carefully.



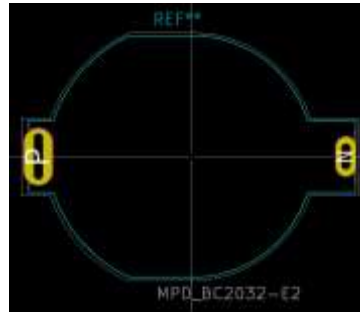


Layout

When you assign a footprint to a symbol, KiCAD attempts to match the symbol pins to the footprint's pads.

In this case, the symbol, which we got from the global built-in library, has pins 1 and 2, which KiCAD attempted to match to the footprint's pads, which are names P and N.

Let's take a quick look at the warnings and errors again.



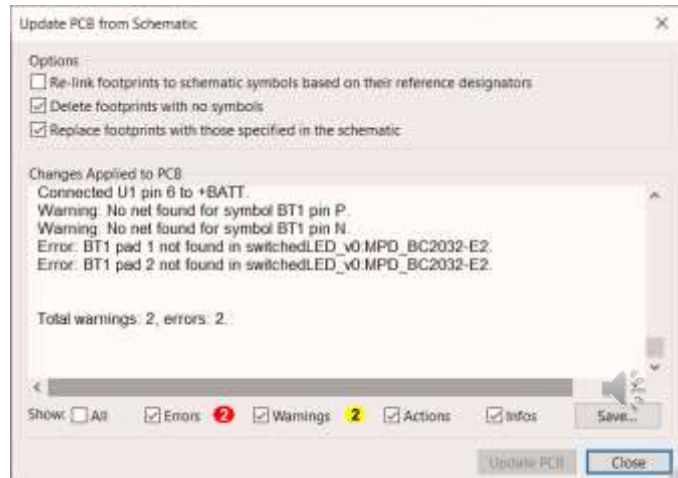


Layout

After linking pins 1 and 2 with pads P and N, KiCAD was looking in the schematic's battery symbol for two pins called P and N because that's what the footprint says they should be called.

Obviously, it didn't find them, and thus there are no nets associated with those pin (because those pins don't exist).

That's the warning - no nets.



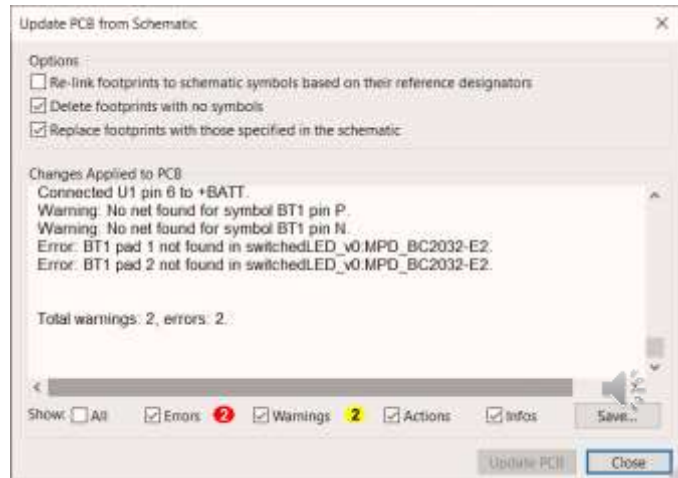


Layout

Similarly, KiCAD went looking for pads 1 and 2 in the footprint because the symbol said those should exist.

Of course, the pads are actually called P and N, so pads 1 and 2 weren't found in the footprint.

Hence, the errors – no pads.

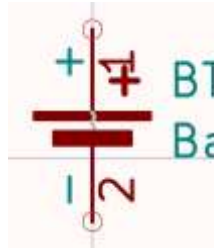




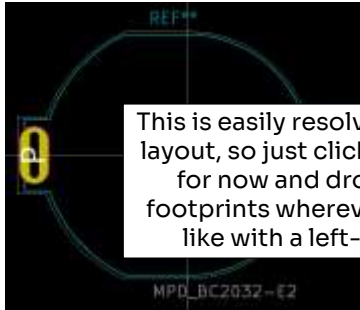
Layout

Recall that I brought this concern up waaaaay back when I said that KiCAD not having devices improved flexibility, but meant you have to be careful about pins.

And now we know – symbol pin numbers must match footprint pad numbers.



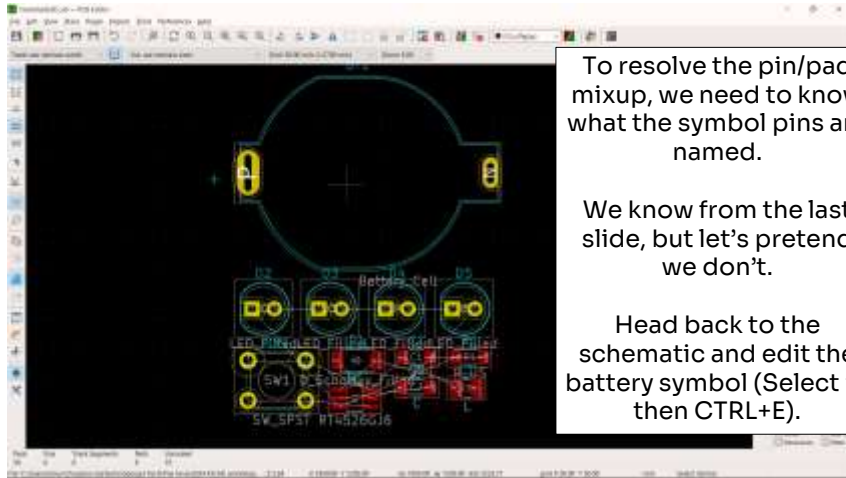
This can be avoided in the future by downloading the symbol along with the footprint, and then using the specific symbol instead. Then they'll be designed to match.



This is easily resolved in the layout, so just click "Close" for now and drop the footprints wherever you'd like with a left-click.



Layout



To resolve the pin/pad mixup, we need to know what the symbol pins are named.

We know from the last slide, but let's pretend we don't.

Head back to the schematic and edit the battery symbol (Select it, then CTRL+E).

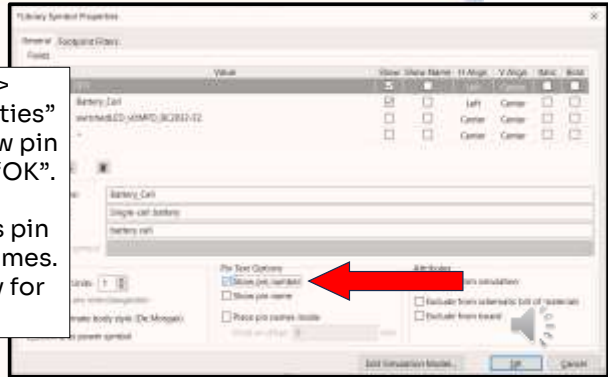


Layout



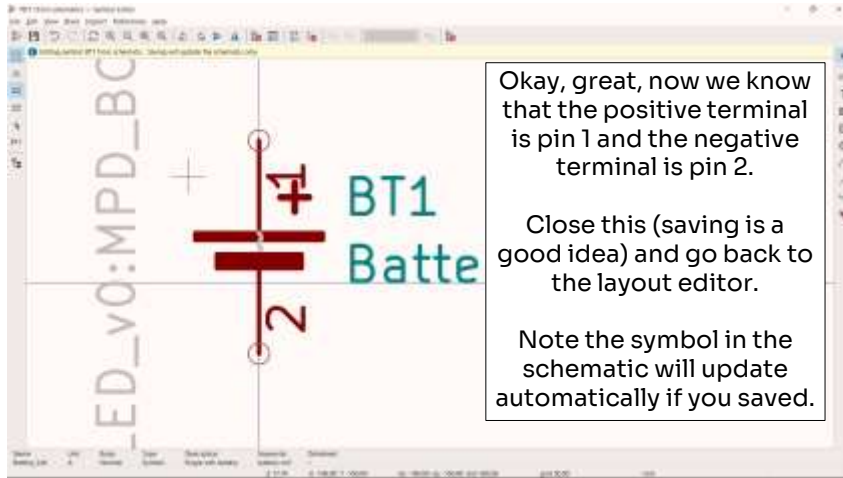
Go to "File" > "Symbol Properties" and check "Show pin number". Click "OK".

KiCAD matches pin *numbers*, not names. Names are only for people.





Layout



Okay, great, now we know that the positive terminal is pin 1 and the negative terminal is pin 2.

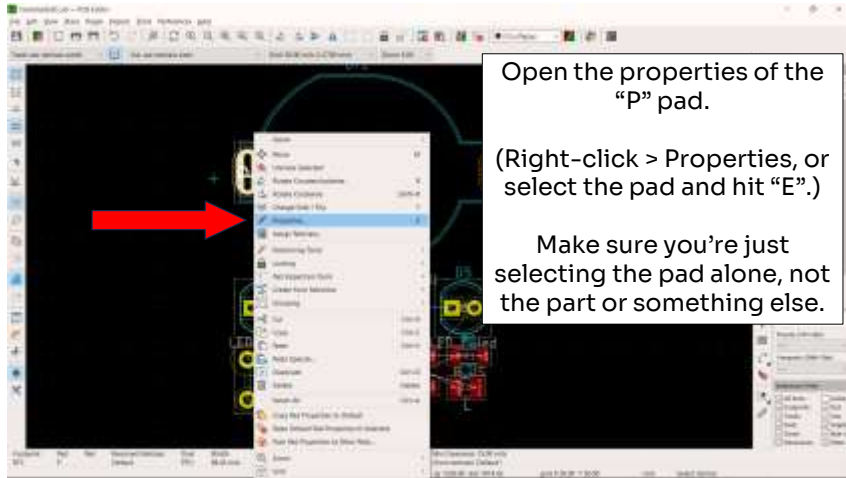
Close this (saving is a good idea) and go back to the layout editor.

Note the symbol in the schematic will update automatically if you saved.





Layout



Open the properties of the “P” pad.

(Right-click > Properties, or select the pad and hit “E”.)

Make sure you’re just selecting the pad alone, not the part or something else.





Layout



Re-number this terminal to "1" rather than "P".

Click OK.

If you notice "Net name" is "<no net>" and are worried, don't be – we'll force that to update in a second here.

Project 87: Battery_Cell, front side, rotated 0 deg

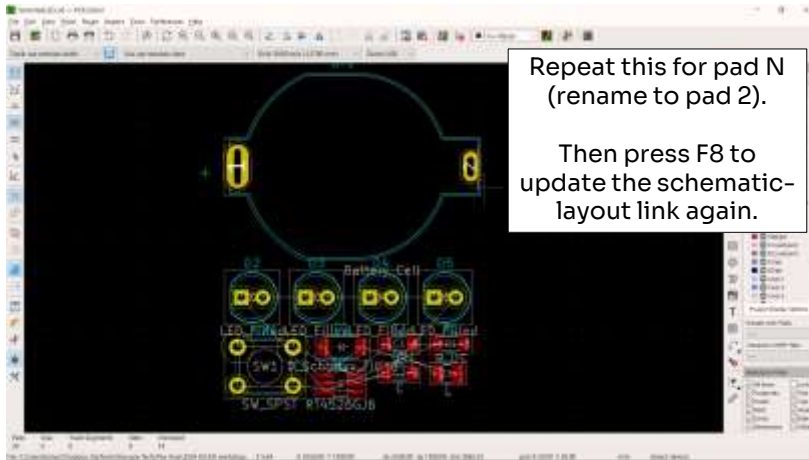
Preview pad in sketch mode

OK Cancel





Layout



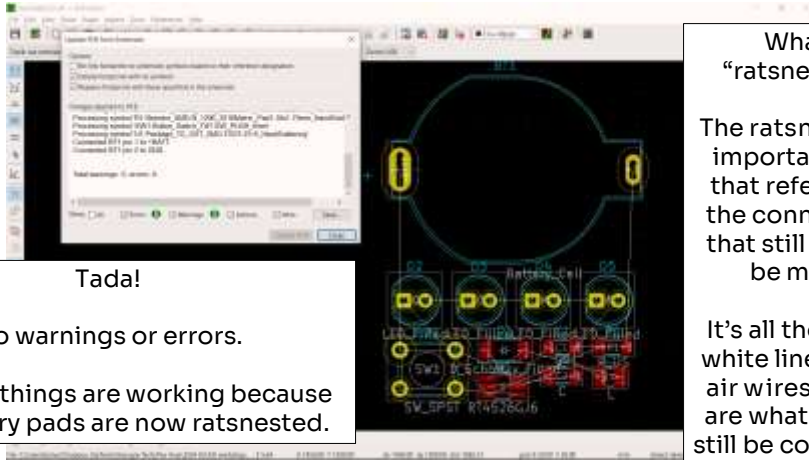
Repeat this for pad N
(rename to pad 2).

Then press F8 to
update the schematic-
layout link again.





Layout



Tada!
No warnings or errors.
We know things are working because
the battery pads are now ratsnests.

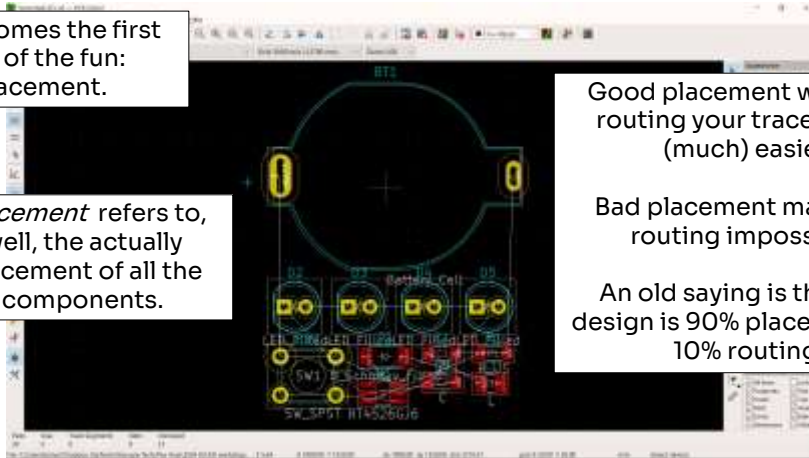
What's
“ratsnests”?
The ratsnest is an
important term
that refers to all
the connections
that still need to
be made.
It's all those thin
white lines called
air wires – those
are what need to
still be connected.



Layout

Now comes the first half of the fun: placement.

Placement refers to, well, the actual placement of all the components.



Good placement will make routing your traces much (much) easier.

Bad placement may make routing impossible.

An old saying is that PCB design is 90% placement and 10% routing.




Layout - Shortcuts

- Go ahead and try placing the components now.
 - Move by click-and-drag or select-and-“M”
 - Rotate with “R”
 - Flip to the other side of the board with “F”.
 - If your component turns red, it means it’s illegally positioned
 - Hold CTRL to get ultra-fine positioning grid
- It may be helpful to hide the fab layers
 - It’s a lot of distracting text.
 - The little “eye” icons on the right under “Layers”
- Next slide has a few more pointers...





Layout – Tips and Tricks

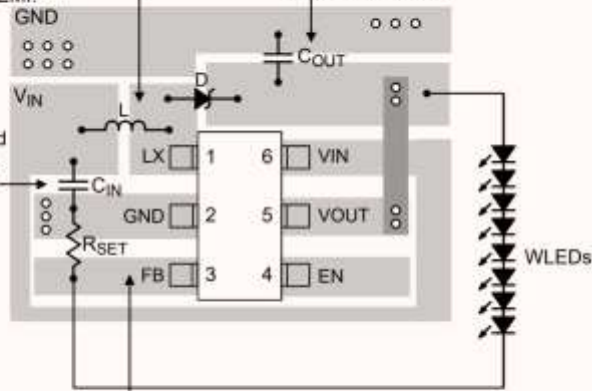
- One thing you may notice is why the net names are so useful. What is “Net-(D1-A)” anyway?
- IC datasheets often have layout recommendations. These can be very helpful because they’re known working arrangements!
- Again, two screens is helpful here.
- Watch the ratsnest as you move parts around.
- Conceptualize how to circuit flows together and cluster related componens.
- Good placement takes time! No need to rush.
- Your layout will very likely not look anything like your schematic, *and that’s okay.* 
 - Remember: the schematic is for people, and the layout is for electrons



The inductor should be placed as close as possible to the switch pin to minimize the noise coupling into other circuits. LX node copper area should be minimized for reducing EMI.

The C_{OUT} should be connected directly from the output schottky diode to ground rather than across the WLEDs

C_{IN} should be placed as close as possible to VIN pin for good filtering.



To save you the trouble of finding the datasheet, here is the recommended layout for the RT4526.

FB node copper area should be minimized and keep far away from noise sources (LX pin) and RS should be as close as possible to FB pin.

I suggest that you paused the video here and take some time to arrange your components. As I mentioned already, placement is most of the work. With good placement comes easy routing. Arranging the IC based on the datasheet's suggestion here is good practice, if possible.



Layout

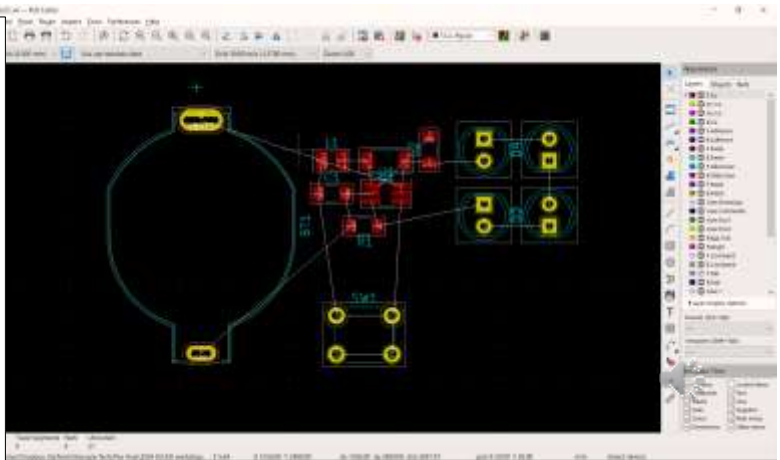
This is MY layout.

It may not be YOUR layout.

And that's okay.

There are many ways to layout a board.

For simple boards, as long as all the connections are made, the rest probably doesn't matter.



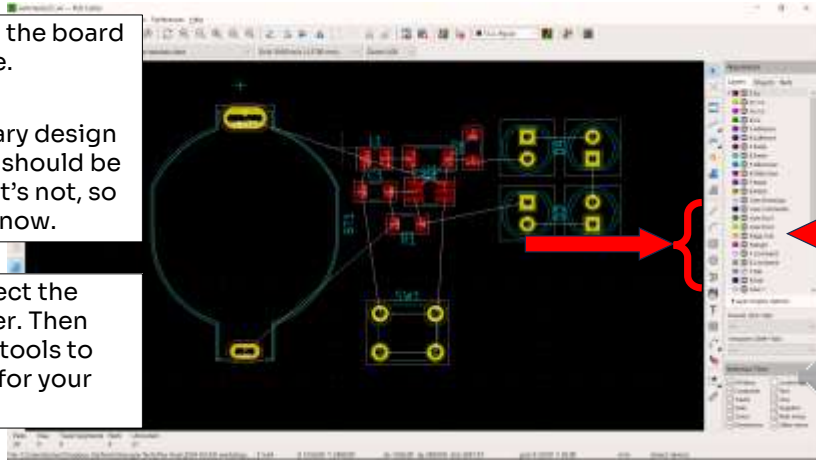


Layout

Next is defining the board outline.

If this is a primary design constraint, this should be done first. But it's not, so we'll do it now.

On the right, select the "Edge-Cuts" layer. Then use the drawing tools to make an outline for your board.

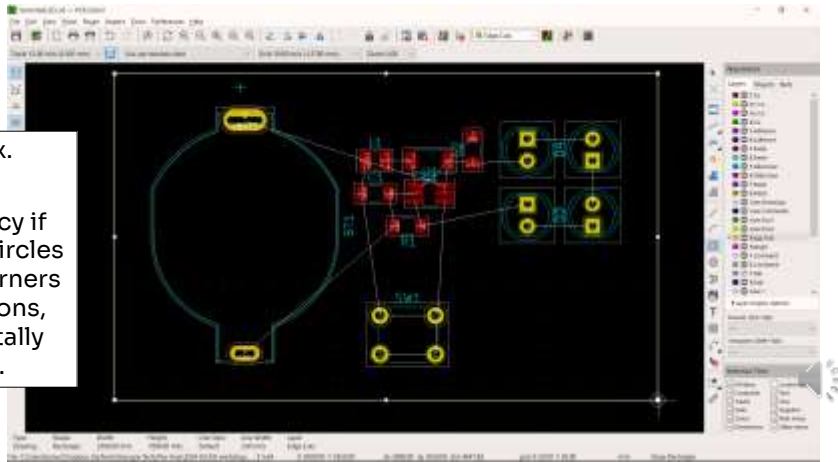




Layout

I made a box.

You can be fancy if you want, with circles and rounded corners or weird polygons, but a box is totally acceptable.



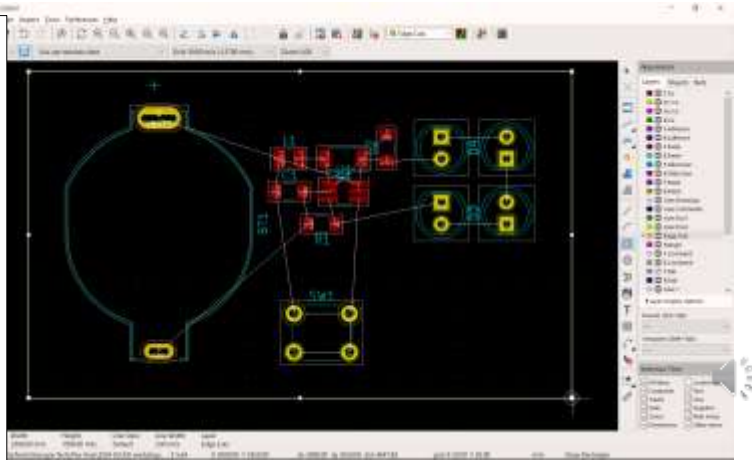


Layout

Next we want to define any large planes (or polygons or pours).

These are copper areas that are completely filled (flooded), and can be connected to a net.

Used widely for ground planes or power planes.



It's safe to think of planes as arbitrarily-shaped traces. Larger traces have lower impedance, so full-board planes have the lowest possible impedance of any possible trace.

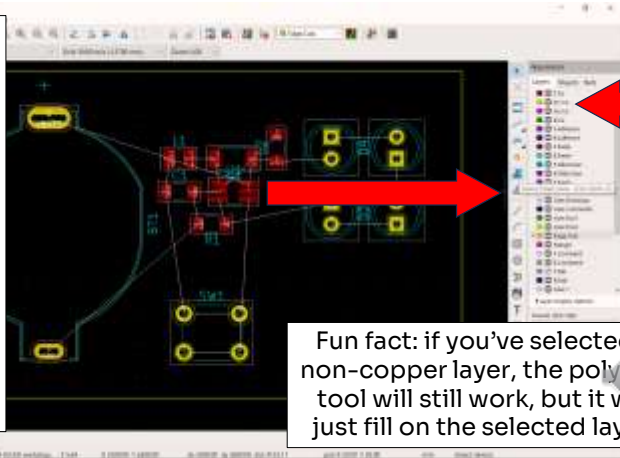


Layout

We're going to make a ground plane. These should cover a full layer of your board to minimize impedance.

We'll use the bottom layer, so select the bottom copper layer (B.Cu) on the right.

Then click the "Add Filled Zone" icon (or CTRL+Shift+Z), and click the top-left corner of your board outline (in yellow).



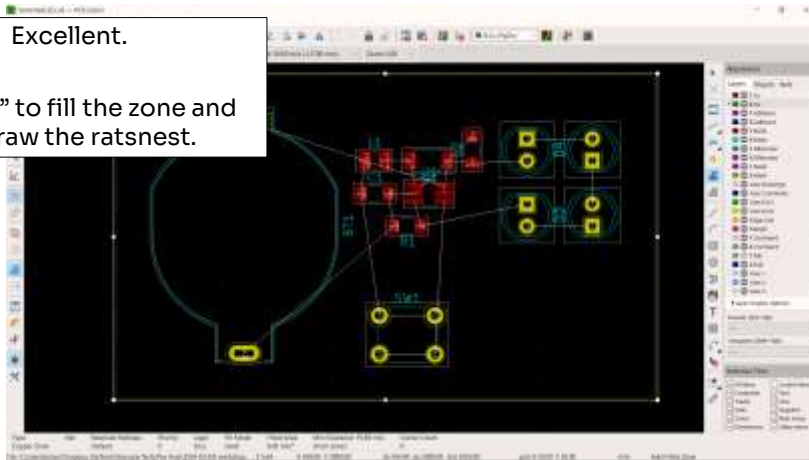
Fun fact: if you've selected a non-copper layer, the polygon tool will still work, but it will just fill on the selected layer.



Layout

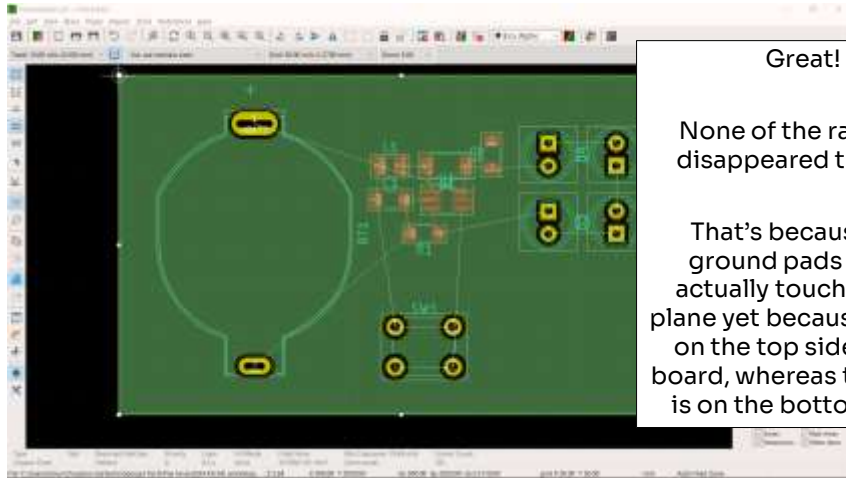
Excellent.

Press "B" to fill the zone and re-draw the ratsnest.





Layout



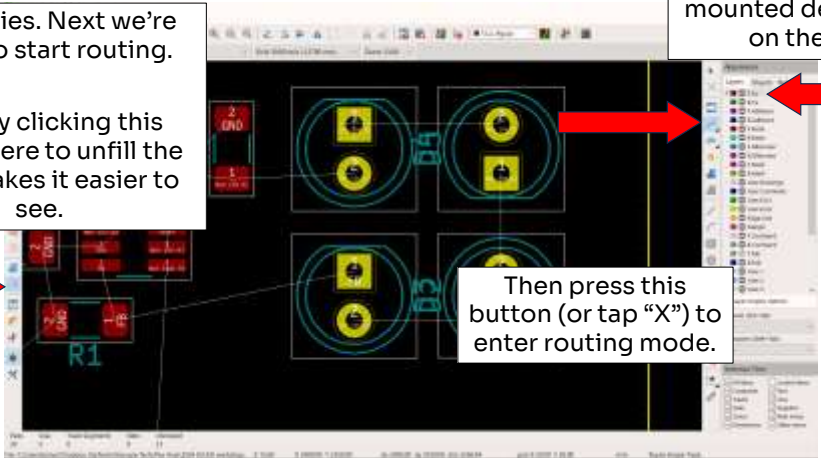
It's also because I made a mistake when generating the zone and set it to "no net" rather than "GND", so the GND pin on the battery should be connected but isn't.



Layout

No worries. Next we're going to start routing.

Start by clicking this button here to unfill the zone. Makes it easier to see.



Select the top copper layer (F.Cu) because that's where we want to run our traces since the surface mounted devices are on the top



Then press this button (or tap "X") to enter routing mode.

Hitting "X" will start a route where you mouse is on the canvas. Hitting the "route" icon will allow you to left-click somewhere to start the route.

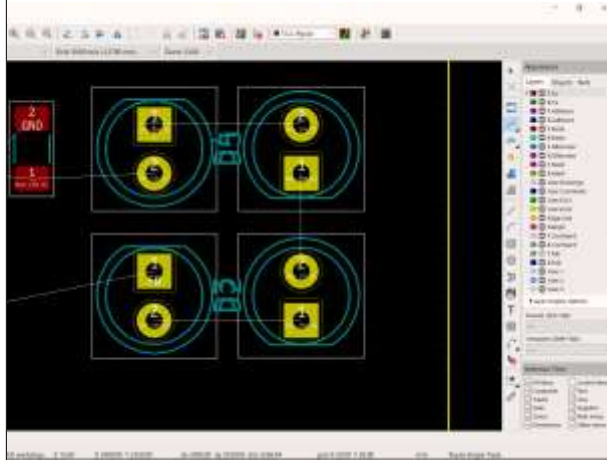


Layout

I'm going to start with the LEDs because they're the simplest.

Just click (don't hold) a pad to start the route, then drag your mouse to the end of the route, and click again to end it.

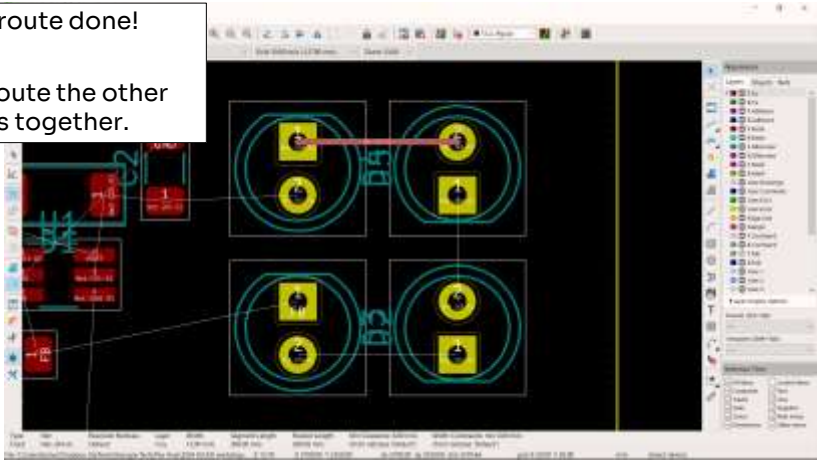
You don't need to follow the ratsnest exactly. That just shows what needs connecting, not always *how* to connect it.





Layout

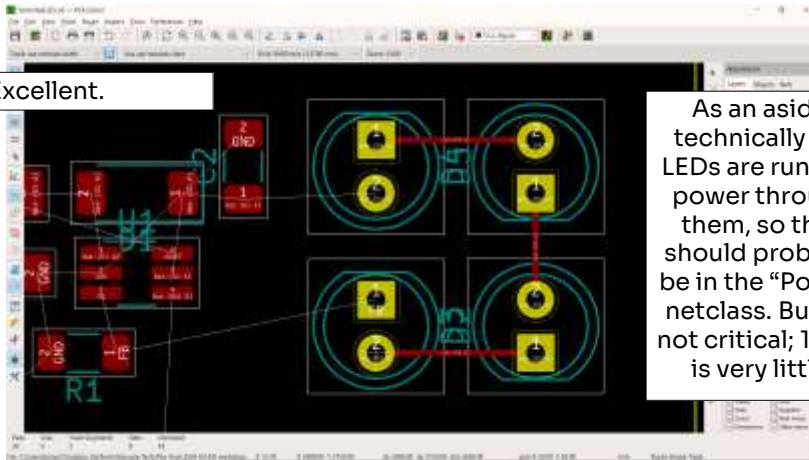
One route done!
Try to route the other LEDs together.





Layout

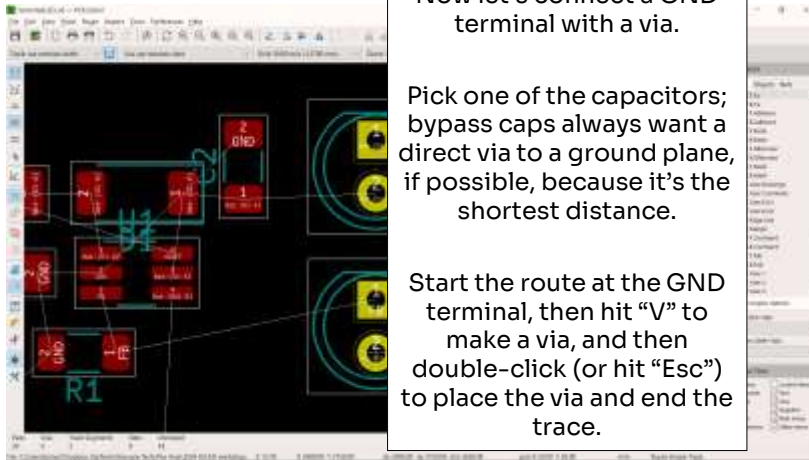
Excellent.



As an aside, technically the LEDs are running power through them, so they should probably be in the "Power" netclass. But it's not critical; 10mA is very little.



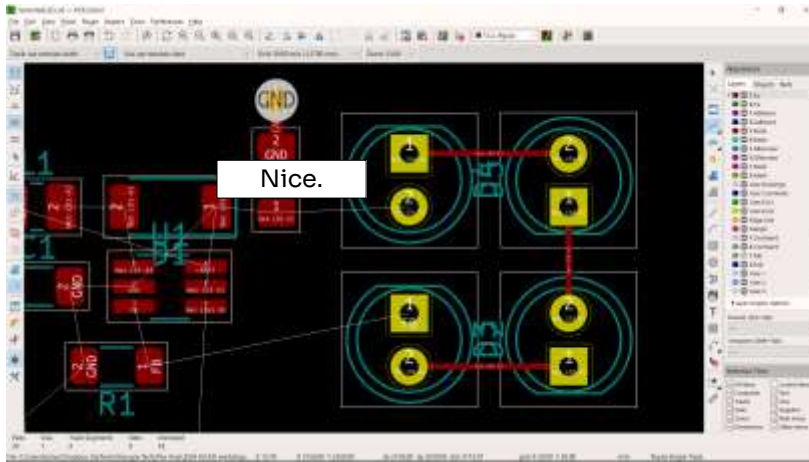
Layout



Not necessary to



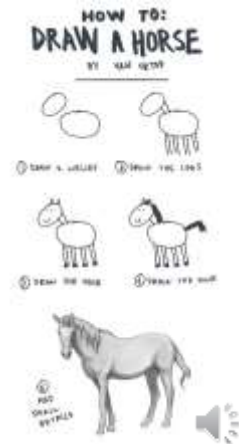
Layout





Layout

- So now it's your turn to complete the layout.
- Hopefully it's not too much like drawing a horse, but the following slides have a few tips.
- Plan to start with the IC, since that arrangement is the most specific.





You don't need multiple vias here because our design isn't that precise.

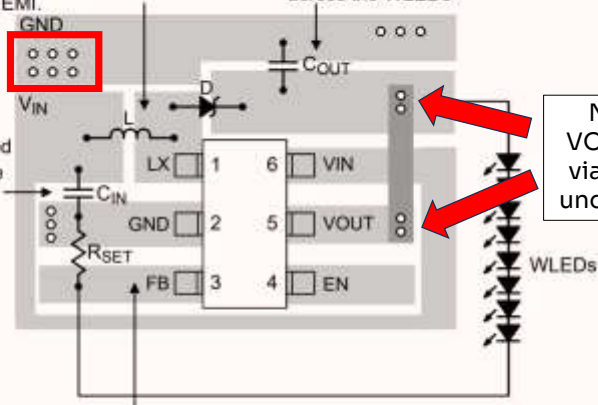
The inductor should be placed as close as possible to the switch pin to minimize the noise coupling into other circuits. LX node copper area should be minimized for reducing EMI.

The C_{OUT} should be connected directly from the output schottky diode to ground rather than across the WLEDs

C_{IN} should be placed as close as possible to VIN pin for good filtering.

Try routing the IC to match the suggested layout from the datasheet.

Note the square traces are just an affectation. Just make the same connections.



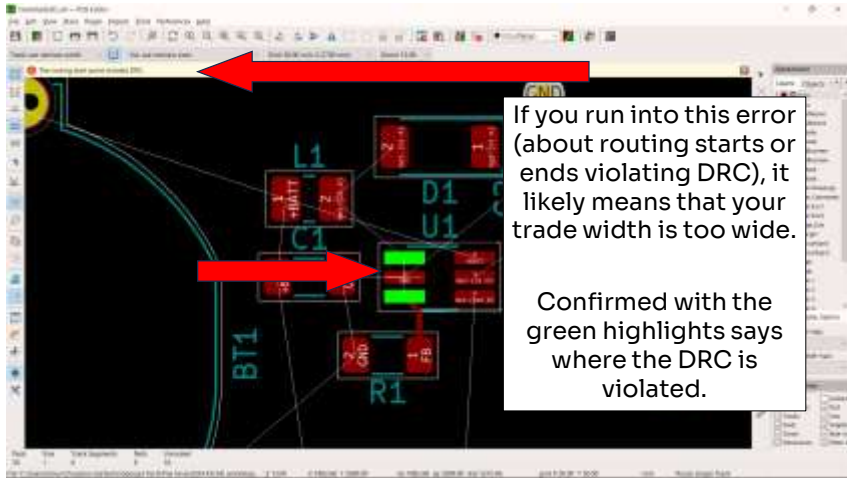
Notice that VOUT's trace is via-connected underneath VIN.

FB node copper area should be minimized and keep far away from noise sources (LX pin) and RS should be as close as possible to FB pin.

(I'll keep this image up later too)

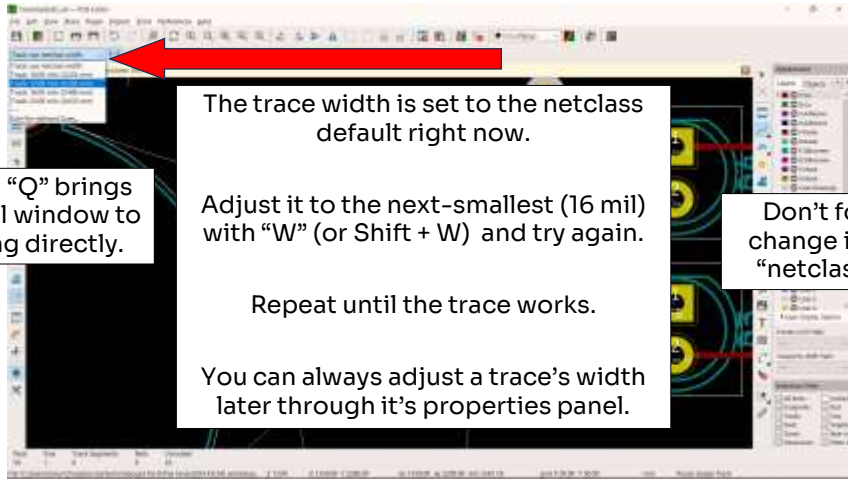


Layout





Layout



Pressing “Q” brings up a small window to set sizing directly.

The trace width is set to the netclass default right now.

Adjust it to the next-smallest (16 mil) with “W” (or Shift + W) and try again.

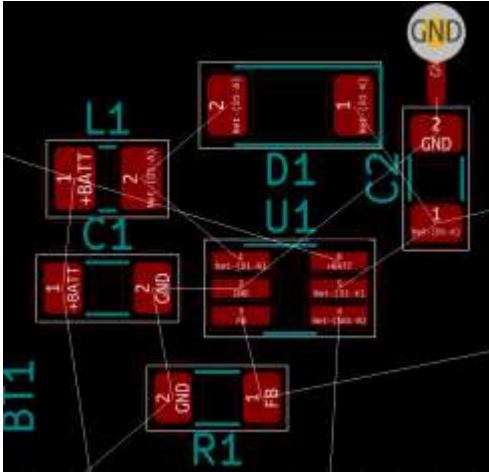
Don't forget to change it back to “netclass” after!

Repeat until the trace works.

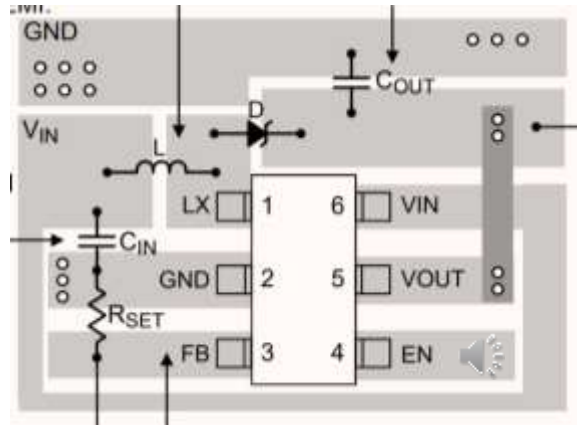
You can always adjust a trace's width later through it's properties panel.



For reference



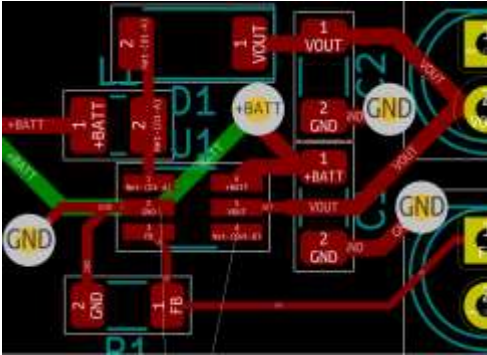
Press “/” to flip the trace’s bend angle.
“D” will drag a trace (better than “M”)



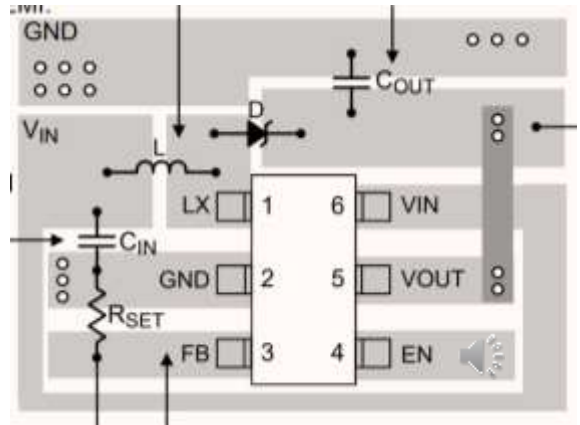
Okay, pause the video here and try to route the IC and its associated components, shown in my layout on the left, like the recommended layout on the right.



Routed!



Not the prettiest routing job ever, but it'll probably work.

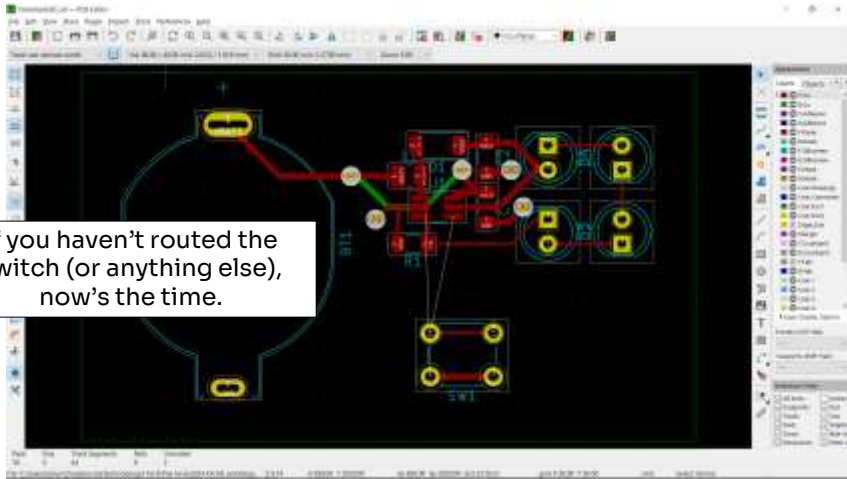


Part of the issue with matching the recommended layout is that our parts are much larger than the layout expectation, so they don't quite fit where the layout expects them.



Layout

If you haven't routed the switch (or anything else), now's the time.

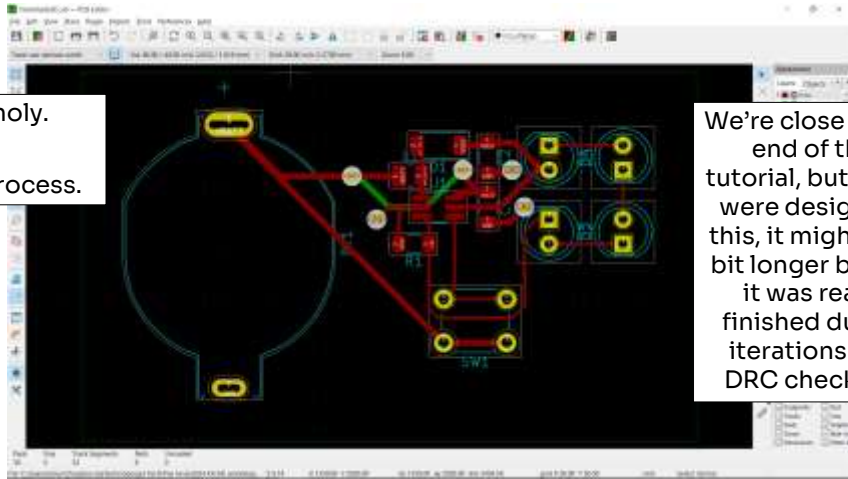




Layout

Holy moly.

What a process.



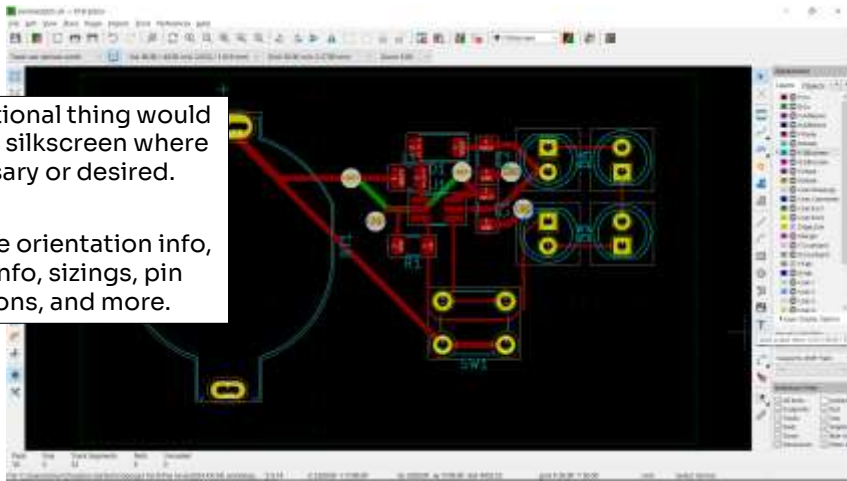
We're close to the end of the tutorial, but if you were designing this, it might be a bit longer before it was really finished due to iterations and DRC checking.



Layout

One additional thing would be to add silkscreen where necessary or desired.

Things like orientation info, usage info, sizings, pin functions, and more.



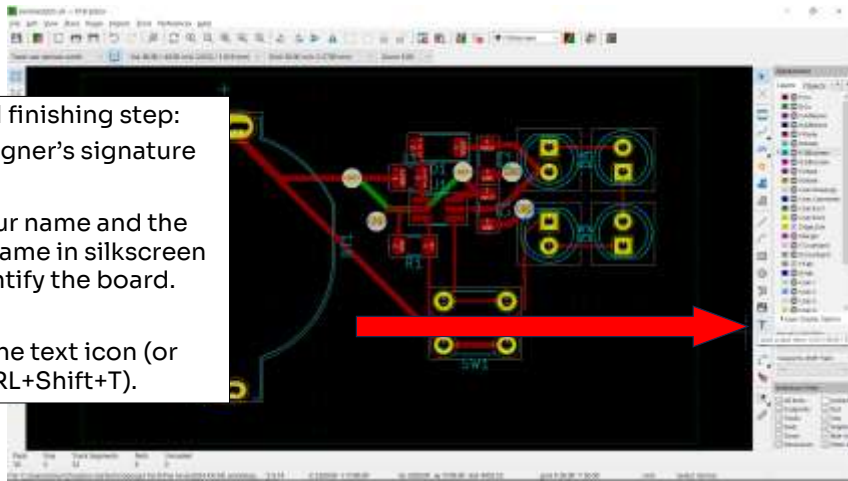


Layout

A small finishing step:
The designer's signature

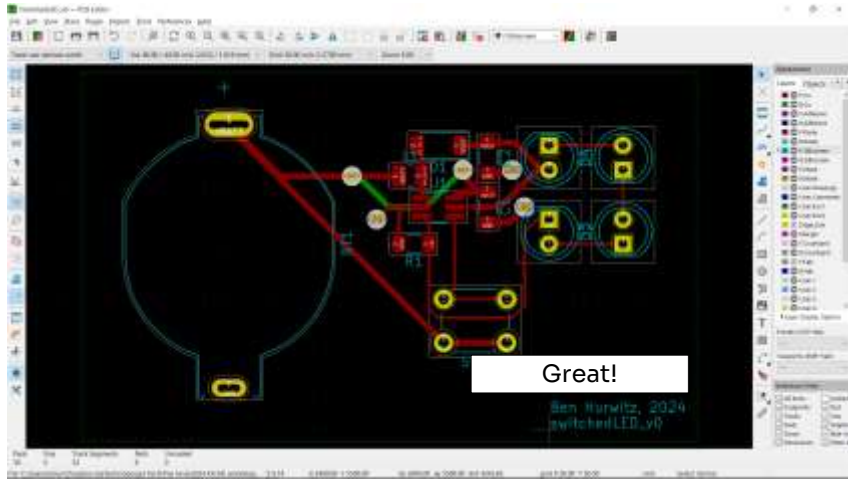
Add your name and the
project name in silkscreen
to identify the board.

Click the text icon (or
CTRL+Shift+T).





Layout





End of Part 5B

And with that, we end part 5B of our PCB design with KiCAD series with a nearly completed layout! All that's left is to check the mechanical dimensions of the various components, the DRC, and plot the gerbers. We'll talk about all that and more in part 5C. A PDF of this video is available as well, linked in the description and hosted on The Hive's Wiki.

See you there.